Radiation Tolerant Source Interface Unit for the ALICE Experiment

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Abstract

The ALICE Detector Data Link (DDL) is a high-speed optical link designed to interface the readout electronics of ALICE sub-detectors to the DAQ computers. The Source Interface Unit (SIU) of the DDL will operate in radiation environment. Tests showed that configuration loss of the Altera APEX II FPGA device used earlier on the DDL SIU card is only marginally acceptable. We developed a new version of the SIU card using Actel ProASIC+ device based on flash memory technology. The new SIU card has been extensively tested using neutron and proton irradiation. In this paper we present the SIU card and describe the results of irradiation measurements.

I. INTRODUCTION

In the data-acquisition (DAQ) system of the ALICE experiment [1], high-speed optical links, so-called Detector Data Link (DDL), will carry detector data from the front-end electronics to the first layer of computers. The DDL can transfer the event fragments at 200 MB/s. The DDL consists of three components: the Source Interface Unit (SIU), the Destination Interface Unit (DIU) and the duplex, multimode optical cable between them. The SIU cards are attached to the readout electronics cards of the detectors. The DIUs will either be integrated on the DAQ Readout Receiver Cards (D-RORCs) or they will be attached to the receiver cards of the High-Level Trigger (HLT) farm. (see Figure 1).

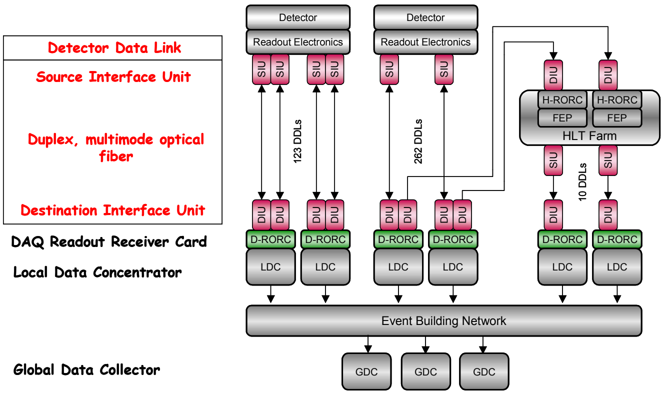

Figure 1: ALICE DAQ/HLT layout

The main function of the link is to provide simple, yet efficient standard interface for every detector in the ALICE experiment. At both interfaces of the link, the interface clock is supplied by the user. It allows the user to use the appropriate clock frequency for the readout. The front-end interface consists of a half-duplex, 32-bit data bus and a few control signals. During the acquisition phase, the interface behaves as a simple synchronous FIFO interface. The architecture of the link is best described as data push architecture, where the transfer, including speed and rate, is controlled by the source. To guarantee the lossless transmission, the DDL uses full duplex flow-control mechanism.

At the level of the physical layer, we are using a bi-directional, high-speed optical link. Using 2.1 Gb/s serial speed, the peak data rate can exceed 200 MB/s. The backward channel allows detector control and/or configuration.

Given the SIU is going to be installed on the detector, it has to tolerate certain level of radiation. This is going to be the main topic of this paper.

II. RADIATION LEVELS IN ALICE

In Table 1 are listed the radiation levels in the detectors where the SIU cards are directly installed on the front-end electronics [2]. The other detectors have the SIUs in shoeboxes, close to the TPC [3] or in racks in the underground area or in one of the counting rooms. According to the latest simulations [4], the highest radiation level for the SIU card is expected at the inner radius of the TPC detector, where the total ionising dose is 1.6 krad and the 1 MeV equivalent neutron fluence is 1.47×10^{11} neutrons/cm^2 for 10 years of operation.

Table 1 Radiation levels in ALICE for 10 years of LHC operation

Detector	Dose [rad/Gy]	n-Φ [n/cm^2]	n-Φ [n/cm^2] 1 MeV n-equ.	h-Φ [n/cm^2] 1 MeV n-equ
TPC (inner)	1600/16	$3.9\text{x}10^{11}$	$1.4\text{x}10^{11}$	$1.5\text{x}10^{11}$
TPC (outer)	220/2.2	$2.5\text{x}10^{11}$	$4.4\text{x}10^{10}$	$4.5\text{x}10^{10}$
TRD	180/1.8	$1.6\text{x}10^{11}$	$2.5\text{x}10^{10}$	$2.6\text{x}10^{10}$
TOF	120/1.2	$1.1\text{x}10^{11}$	$1.9\text{x}10^{10}$	$2.0\text{x}10^{10}$
HMPID/PHOS	50/0.5	$8.6\text{x}10^{10}$	$1.7\text{x}10^{10}$	$1.7\text{x}10^{10}$

III. RADTOL MEASUREMENTS OF THE SIU COMPONENTS

The SIU hardware consists of three main, and several auxiliary components. The full-duplex optical transceiver makes the conversion between the optical serial data and the high-speed differential electrical data. The electrical transceiver performs serial-to-parallel and parallel-to-serial data conversion. The DDL protocol and additional logic functions are implemented in a programmable logic device (FPGA).

The radiation tolerance tests of the main components have been done in the framework of the DDL Radtol Project. The project is a collaboration between CERN, RMKI – KFKI and its partners in Hungary (Cerntech, TU Budapest). It was born in 1998 to cover all radiation related issues of the DDL. The radiation tolerant measurements of the SIU components and the prototype SIU card done till 2004 are described in details in [5].

According to the above measurements the auxiliary components of SIU card (crystal oscillators, voltage regulators) and several electrical and optical transceivers have successfully passed the tests: the rate of the functional or transmission errors induced by radiation is below the permitted error rate.

We also tested the “heart” of the SIU card: the programmable logic device (FPGA). Two devices from the two major SRAM-based FPGA vendors have been tested: the Altera APEX-E device (EP20K60E) and a Virtex II device from Xilinx. The APEX-E device was used on the prototype DDL cards, while the Xilinx Virtex II device was mounted on an evaluation board. Tests have shown that these devices tolerate the required level of total ionisation dose (TID). So, in our tests we focused on two different effects: the single event upsets (SEUs) in the user logic and in the device configuration.

The loss (or corruption) of the device configuration (i.e. configuration cell changes its state due to high-energy particle interacting with the device) is very critical, because it causes a functional interrupt (FI) on the given device. According to the tests we have calculated MTBF value and found that we should expect 1 loss of configuration every hour in the DAQ system containing 400 DDL SIUs.

Therefore, it has been decided to redesign the DDL card. Last year, we presented three possible solutions to the ALICE collaboration. Amongst them, two solutions are based on SRAM-based FPGAs, which support different mitigation techniques, such as configuration error detection and device reconfiguration during operation. However both of these solutions require additional circuits on the board. The third solution, is based on a different silicon technology, the so-called flash-memory based FPGA produced by Actel. This type of programmable logic device seems to combine the power of the FPGAs and the intrinsic resistance against radiation effects seen in other type of FPGAs.

IV. THE NEW SIU CARDS

For the new DDL card, we have selected the ProASIC family from Actel. This choice has several advantages. Every irradiation test we have done so far, shows good performance. In the ProASIC device family, users can find devices with size from 75 K gates up to 1 M gates, which is more than enough for the implementation of the DDL SIU functions (reminder: the actual Altera device is claimed to have 160 K gates). It consumes less power, without peaks observed during power-on phase of the SRAM-based devices. It can be explained by the fact that the ProASIC device does not require configuration at power-up, which makes it a so-called instant-on device. The non-volatile configuration cells will also eliminate the need of an external configuration memory (price). At the time of the card development only AP150 device was available from the ProAsic family. Actel announced the new generation of their flash-based FPGA devices, the ProASIC3 family. The new family will provide higher performance at lower power consummation, and lower price. According to the vendors information we can expect approximately factor of two increase in the clock frequency. The new device is available from September 2005. The two device families are pin-compatible. We have designed the SIU PCB to suit both of them.

The only disadvantage of choosing ProASIC came from the fact that it is based on a different architecture. As such, it requires different software tools for development. Because the internal performance is worse than SRAM-based FPGAs, we had to re-engineer the timing critical modules (framing / de-framing at 110 MHz). The architecture of the ProASIC provides less internal resources (e.g. high-speed clock network) and less complex logic elements. In order to alter the content of the flash memory cells inside the device, that is to change the device configuration, we need to use special voltages (+16 V and –13.8 V). This will make practically impossible to perform remote device configuration.

The first prototypes of the radiation tolerant SIU contains Actel APA150 device (see Figure 2).

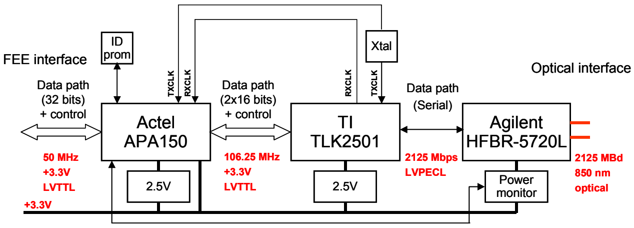

Figure 2: Radtol SIU block diagram

As for the SIU firmware, we ported the modules from the Altera DDL firmware. The timing critical modules have been reengineered and optimised. The complete firmware had been simulated. The card was tested using DDL software utilities, both in CERN and in KFKI – RMKI in Budapest. At the same time long-term test have been executed using DATE, the ALICE DAQ software.

V. IRRADIATION TESTS OF ACTEL PROASIC+ AND SIU CARDS

We carried out several series of tests to investigate the configuration loss of the Actel ProASIC+ device in radiation environment. For the tests, we have used the new DDL SIU card and an evaluation board from Actel. The first series of measurements took place at TSL, (Uppsala, Sweden) using protons at energy of 171 MeV, 94 MeV and 48 MeV. Further series of measurements were done at ATOMKI (Debrecen, Hungary) using thick target p+Be neutrons with spectrum extending up to En=14 MeV.

Neither the ProASIC+ evolution board nor the SIU board showed any configuration loss in proton and neutron irradiations.

However, the SIU card provoked a link down after the equivalent of 5 years of irradiation (10^{11} n/cm^2). This error can be explained by a SEU in one of the state-machines responsible for the link management. The problem could be fixed by cycling the power on the card.

To investigate the probability of link failures and transmission errors in radiation environment we have developed two special test scenarios. During the first one, the SIU was put in test mode. Short data blocks were sent to SIU (put into the radiation area) via the DDL link. The SIU firmware has sent the data back. We have reset the link intentionally in every second. Errors have been detected during about every eight hundredth link re-initialisation: the SIU has stuck in power-on reset state. The link initialisation error could be fixed remotely in every case.

During the second test scenario the SIU in radiation environment received data blocks form front-end simulator (this is the normal operation mode). The SIU firmware has sent the blocks to the DIU and RORC via the DDL link. In this case we have detected only data errors. The tests have shown that we can expect one bit error every 4 hours in the DAQ system containing 400 DDL SIUs. During normal operation this will not be detected.

VI. CONCLUSION

Using the Actel ProASIC+ based SIU in radiation environment we have not found any configuration loss. On the other hand we have found that the probability of transfer errors (and link failures in the case of frequent link reset) was similar to the probability of the configuration loss of the SRAM-based FPGA devices. First of all the power-on reset state machine should be improved, to avoid being stuck in a state. This can be done by redesigning the firmware.

Secondly, we have to find out the reason of the data errors: whether the SEUs were produced in the embedded FIFO memories or in the register cells of the FPGA. After finding the source of these errors, we can work out the adequate mitigation techniques. In order to detect errors in the memory cells, we can use the built-in parity checks of the device. To handle errors present on the data path inside the device, we might extend the CRC for the whole data path, or use triple module redundancy, wherever it is appropriate. Therefore, we are now developing special firmware and software (for both the ProASIC+ and the ProASIC3 devices) and we continue the radiation tests.

VII. ACKNOWLEDGEMENT

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VIII. REFERENCES

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