

Proposal for the final SIU

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1. Introduction

The prototype of the Source Interface Unit (SIU) of the Detector Data Link (DDL) has been developed according to the DDL User Requirements Document (URD) [1]. The first prototype links have been tested thoroughly and the integration with the read-out system prototypes of the different detectors started this year. Meanwhile, some of the user requirements have been changed (e.g. the size restrictions). At the same time, significant evolution happened on the electronic component market, which must be taken into account for the final interface specification of the DDL. Finally, since the number of links in the final system is substantial (about 400), it is essential to choose the cheapest possible solutions.

In respect to these changes, we now propose modifications to the specification of the SIU. The proposal is based on the results of the previous design work, and the everyday experiences we face using the prototypes. The proposal covers three main points, the size and form factor of the SIU board, the SIU interface connector, and the signal voltage levels of the interface.

If the proposed changes are accepted, it will be possible to use up-to-date components and solutions in the hardware design. This will eliminate difficulties raised by the present user requirements, build cheaper cards with better yield, and possibly design a common PCB for the SIU and the DIU configuring them as a source or a destination interface unit by the firmware.

2. SIU size and form factor

According to the original requirements, the SIU should have a footprint of less than 50 cm². In case of the ITS-Pixel and ITS-Drift sub-detectors, the required size was less than 15cm². Since they decided to use other solution to read out their detectors, the later requirement has become needless. Meanwhile, several sub-systems (e.g. TPC detector) required more standardized form factor for the cards.

The first version of the SIU has been designed and manufactured. The dimensions of the board are 80 x 35 x 13 mm (28 cm²). This was a challenging step toward the very strict size requirements of that time. In order to fit in the small size we had to choose special components with FBGA packages and

the PCB had to be designed to use special techniques, such as filled via holes, etc. During the manufacturing of the board and the mounting of the components, we faced many difficulties and in particular a low yield of good boards after mounting. Although these difficulties could be solved, this requires extra efforts, time and money. Now having more relaxed requirements on the size, we have the possibility to design a board, which eliminates the unnecessary difficulties.

Accordingly, we propose a new form factor based on the Common Mezzanine Card (CMC) [2] format. The CMC form factor is widely used in embedded and industrial applications. The standard provides the mechanics for mezzanine cards, while it keeps the possibility to specify custom interfaces for the cards. The new form factor will allow an easy integration into the different sub-systems.

Due to the existing size constraints, however, it would not be possible to use the single CMC board size directly, as it would be too large as SIU form factor. Therefore, we propose to adopt about the half of that instead. The main dimensions of such card are 149 x 40 x 10 (mm). One should note that the optical connector would protrude through the edge of the card. The heights of the components placed on the board shall conform to the envelope specified by the standard. See figure 1 for details.

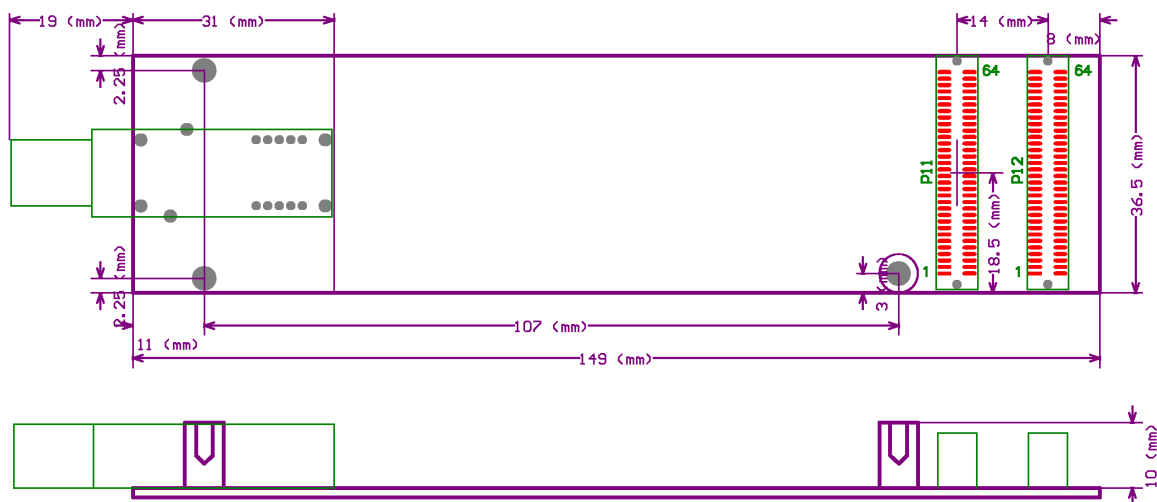


Figure 1 Mechanical drawing of the common link card

3. SIU interface connector

The SIU interface provides a half-duplex bus with control signals for the FEE cards. In addition, it contains the standard JTAG TAP signals. Beside these signals, the power is supplied to the SIU through the interface connector. The actual connector of the prototype SIU was chosen according to the very small board size. For details of the interface specification, see the hardware guide [3].

In order to be compatible with the CMC specification we have to change the connector and the pin assignment. The new connectors would host the previous signals; there would not be any change in the interface signal definitions. The standard contains the detailed description of the connector, which is defined by the EIA standard (EIA E700 AAAB).

The pin assignment of the new SIU (Figure 2) would conform to the CMC specification. However, there are some signals, specified by the standard, which would not be used on the board.

Pins marked with V(I/O) should be tied to +3.3V in any case. The card would use only the +3.3V power supply. The +5V, +12V and -12V power pins would not be connected on the SIU. The reserved signals should be left unconnected.

CMC SIU (P11 connector)

| | | | |
|----|----------------|---------|----|
| 1 | FIBEN_N | -12V | 2 |
| 3 | GND | FILF_N | 4 |
| 5 | FOBSY_N | FIDIR | 6 |
| 7 | BUSMODE1# | +5V | 8 |
| 9 | FBCTRL_N | FBTEN_N | 10 |
| 11 | GND | FBD0 | 12 |
| 13 | FOCLK | GND | 14 |
| 15 | GND | FBD1 | 16 |
| 17 | FBD2 | +5V | 18 |
| 19 | V(I/O) (+3.3V) | FBD3 | 20 |
| 21 | FBD4 | FBD5 | 22 |
| 23 | FBD6 | GND | 24 |
| 25 | GND | FBD7 | 26 |
| 27 | FBD8 | FBD9 | 28 |
| 29 | FBD10 | +5V | 30 |
| 31 | V(I/O) (+3.3V) | FBD11 | 32 |
| 33 | FBD12 | GND | 34 |
| 35 | GND | FBD13 | 36 |
| 37 | FBD14 | +5V | 38 |
| 39 | GND | FBD15 | 40 |
| 41 | FBD16 | FBD17 | 42 |
| 43 | FBD18 | GND | 44 |
| 45 | V(I/O) (+3.3V) | FBD19 | 46 |
| 47 | FBD20 | FBD21 | 48 |
| 49 | FBD22 | +5V | 50 |
| 51 | GND | FBD23 | 52 |
| 53 | FBD24 | FBD25 | 54 |
| 55 | FBD26 | GND | 56 |
| 57 | V(I/O) (+3.3V) | FBD27 | 58 |
| 59 | FBD28 | FBD29 | 60 |
| 61 | FBD30 | +5V | 62 |
| 63 | GND | FBD31 | 64 |

CMC SIU (P12 connector)

| | | | |
|----|-----------|-----------|----|
| 1 | +12V (1) | TAP_TMS | 2 |
| 3 | TAP_TDI | TAP_TDO | 4 |
| 5 | TAP_TCK | GND | 6 |
| 7 | GND | TAP_TRST | 8 |
| 9 | - | - | 10 |
| 11 | BUSMODE2# | +3V | 12 |
| 13 | - | BUSMODE3# | 14 |
| 15 | +3.3V | BUSMODE4# | 16 |
| 17 | - | GND | 18 |
| 19 | - | - | 20 |
| 21 | GND | - | 22 |
| 23 | - | +3.3V | 24 |
| 25 | - | - | 26 |
| 27 | +3.3V | - | 28 |
| 29 | - | GND | 30 |
| 31 | - | - | 32 |
| 33 | GND | - | 34 |
| 35 | - | +3.3V | 36 |
| 37 | GND | - | 38 |
| 39 | - | GND | 40 |
| 41 | +3.3V | - | 42 |
| 43 | - | GND | 44 |
| 45 | - | - | 46 |
| 47 | GND | - | 48 |
| 49 | - | +3.3V | 50 |
| 51 | - | - | 52 |
| 53 | +3.3V | - | 54 |
| 55 | - | GND | 56 |
| 57 | - | - | 58 |
| 59 | GND | - | 60 |
| 61 | - | +3.3V | 62 |
| 63 | GND | - | 64 |

Figure 2 Pin assignment of the new SIU

4. Signal voltage levels

The question of the interface voltage levels is independent from the board size and the interface connector. The proposal of the voltage levels on the interface is based on the evolution of the power supply voltage and signal voltage specifications of today's high performance digital circuits. In the recent years, the speed and the complexity of the digital ICs increased impressively. For this development, it was necessary to reduce the power supply voltages of the integrated circuits. Today's digital ICs, including the programmable logic devices do not need 5V, but 3.3V power supply. Most PLD circuits need lower voltages (2.5V, 1.8V or 1.5V), too, to supply the core logic of the device. These changes in the supply voltages determine the voltage levels of the I/O drivers of the devices as well. Up to now, Low-Voltage TTL (LVTTTL, 3.3V TTL) is the most widely used signalling environment. Only very expensive and special versions of the PLD circuits remain compatible with the old, 5V standards. Most of them, including those that are the best in performance and cost, do not accept 5V TTL signals any more. On the other hand, their LVTTTL outputs can still drive 5V TTL inputs.

The DDL URD specifies two different supply voltages for the SIU, 5V and 3.3V. The present version of the SIU does not use 5V, however, it can accept signals driven by 5V TTL compatible devices. It would be very important for the further development of the SIU cards that the next versions do have a pure 3.3V, LVTTTL signal interface without 5V input compatibility. This change is necessary for using modern PLD circuits (that are not 5V compatible any more) and other effective solutions in the hardware development. This change requires that the cards be driven only with LVTTTL (3.3V) signals.

Any lower voltages that may be required by the components of the SIU will be generated on the board.

5. Summary

A new format of board and new connectors are proposed for the SIU. The changes are motivated by the new user requirements, which allow a larger boards size being implemented at lower cost. In addition, it opens the great opportunity of designing the same PCB for the DIU and SIU, resulting in further cost reduction. It also eases the work in several fields (less design work, more reusable design elements, cheaper prototyping, better components management, easier testing, flexibility of using cards on stock, easier replacement in case of faults, etc).

Change of the voltage level on the DDL interface is required because the modern PLD circuits are not compatible with the 5V TTL signalling environment anymore. The link card should be supplied with 3.3V only and it shall provide LVTTTL compatible signals to the interface.

References

- ¹ G. Rubin, P. Vande Vyvre, "ALICE Detector Data Link (DDL) – User Requirements Document", ALICE-INT-1996-42
- ² IEEE, "Common Mezzanine Format (CMC)", IEEE-1386
- ³ G. Rubin, Cs. Soos, "ALICE DDL – Hardware Guide for Front-end Designers", ALICE-INT-1998-21